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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,405	02/09/2004	Hiroshi Yoshigi	ASAM.0110	6609
7590	04/17/2007		EXAMINER	
Stanley P. Fisher Reed Smith LLP Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042-4503			BANGACHON, WILLIAM L	
			ART UNIT	PAPER NUMBER
			2612	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/17/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)
	10/773,405	YOSHIGI ET AL.
	Examiner	Art Unit
	William L. Bangachon	2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 March 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 5,6 and 10-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 5,6 and 10-15 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input checked="" type="checkbox"/> Other: <u>Examiner's comments</u> . |

DETAILED ACTION

Response to Arguments

1. The Declaration of One Skilled in the Art was received on 3/22/2007. Further, the declaration has been fully considered but they are not persuasive as follows:

Response to Arguments

2. Applicant's arguments filed 03/22/2007 have been fully considered but they are not persuasive.

3. In response to applicant's argument that "the cited references fail to teach or suggest such a "first capacitor 7 (1) connecting between an IC chip 3 and said antenna coil 1 in series, and (2) having a capacitance C1 smaller than an input capacitance Cin 3A of said IC chip 3 such that a reactance of the antenna, the capacitance of the fist capacitor 7 and the input capacitance of the IC chip 3 determine a resonant frequency of the contactless identification according to the invention" [see Remarks, page 2, 3rd paragraph], **a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.** In this case, de Vall was shown to teach of an equivalent L'C' series circuit as claimed, in the form of an IC chip (20), wherein one terminal of the IC chip is connected to the antenna coil (L') through the first capacitor, wherein the antenna coil, the first capacitor

and the IC chip are connected in series as shown in Figure 3b. At this point, de Vall teaches an equivalent circuit as claimed, including an intended use. That is, the capacitor C' and coil L' forms a series resonant circuit {see de Vall, col. 4, lines 31-35+}. With de Vall In view of Mathieu and Stan Gibilisco, it was shown that the capacitor C' in de Vall can be made smaller than an input capacitance of the IC chip (20). Therefore, since the cited prior art is shown to be performing the intended use, then it meets the limitations in claim 5. See MPEP 2114.

4. In response to applicant's argument [see Remarks, page 3, 1st paragraph] that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this instance, de Vall does not disclose "the first capacitor has a capacitance smaller than an input capacitance of the IC chip". Mathieu, in the same field of endeavor, teaches that the input capacitance introduced by an IC chip in the manufacture of tags/transponders is inherent {see Mathieu, col. 1, lines 32-37+}. de Vall shows in Figs. 3a and 3b that resonating circuits can be either series or parallel. Mathieu describes that as the input capacitance of the chip (CS1 in Fig. 5) gets smaller and smaller, a capacitance value CS2 obtained with the screen-printed capacitor 52 is added to compensate (so the overall capacitance stays the same) {see Mathieu, col. 4,

lines 22-33+}. Mathieu suggests that it is advantageous to compensate the input capacitance of the chip in order to obtain perfect resonance. And, with the compensating capacitor on the outside of the chip, perfect resonance can be obtained without having to modify the fabrication process {see Mathieu, column 4, lines 50-55 and paragraph-bridging cols. 4 and 5}. The particular design used by Mathieu is a parallel resonating circuit. With parallel circuits, the total capacitance is $CS_1 + CS_2$ {See Teach Yourself Electricity and Electronics, 2nd Edition, by Stan Gibilisco, page 203}. As CS_1 gets smaller, CS_2 has to get larger to compensate. In a series circuit, the relationship between the two capacitors is $1/CS_2 + 1/CS_1$ {See Teach Yourself Electricity and Electronics, 2nd Edition, by Stan Gibilisco, page 202}. As CS_1 gets smaller, CS_2 must also get smaller to compensate. Therefore, the series relationship is inverse to the parallel relationship. As Mathieu discloses a large capacitor is needed to compensate for the chip capacitor getting smaller {see Mathieu, col. 4, lines 31-33+} and de Vall discloses that either a parallel or series resonator can be used, it would have been obvious to one of ordinary skill in the art, at the time of applicant's invention, to use a series resonator in place of the parallel resonator disclosed by Mathieu because, as taught by Mathieu, the input capacitance of the chip should be compensated in order to obtain perfect resonance. Once this replacement is done, it is inherent that first capacitor C' be smaller than the input capacitance of the IC chip to achieve the same effect (i.e. perfect resonance). Also see Stan Gibilisco, pages 318-319.

5. In response to applicant's argument [see Remarks, page 3, 3rd paragraph] that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Mathieu is cited to teach, "as the input capacitance of the chip (CS1 in Fig. 5) gets smaller and smaller, a capacitance value CS2 obtained with the screen-printed capacitor 52 is added to compensate (so the overall capacitance stays the same)" {see Mathieu, col. 4, lines 22-33+}. Mathieu suggests that it is advantageous to compensate the input capacitance of the chip, and with the compensating capacitor on the outside of the chip, perfect resonance can be obtained without having to modify the fabrication process {see Mathieu, column 4, lines 50-55 and paragraph-bridging cols. 4 and 5}.

Finally, contrary to applicant's argument [see Remarks, page 3, last paragraph] it has now been shown that the cited references and their combinations suggests each and every feature of the present invention as recited in at least independent claim 5. As such, the rejection of claims 5-6 and 11-15 are maintained in this Office action.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 5-6 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over USP 5,608,417 (hereinafter 'de Vall') in view of USP 6,522,308 (hereinafter

'Mathieu'), and further in view of Teach Yourself Electricity and Electronics, 2nd Edition, by Stan Gibilisco.

In claim 5, de Vall teaches of a transponder (considered as functionally equivalent to the claimed contactless identification) comprising:

an antenna copper coil (L') {see de Vall, Figure 1, 4 or 6} formed on the opposite surfaces of a Fleximide substrate (i.e. base) in generally rectangular spirals, considered as functionally equivalent to the claimed metallic vortex pattern {see de Vall, col. 3, lines 31-33+, lines 45-50+};

a first capacitor (C'); and

an IC chip (20), wherein one terminal of the IC chip is connected to the antenna coil (L') through the first capacitor, wherein the antenna coil, the first capacitor and the IC chip are connected in series as shown in Figure 3b. The capacitor C' and coil L' forms a series resonant circuit {see de Vall, col. 4, lines 31-35+}.

de Vall does not disclose "the first capacitor has a capacitance smaller than an input capacitance of the IC chip". Mathieu, in the same field of endeavor, teaches that the input capacitance introduced by an IC chip in the manufacture of tags/transponders is inherent {see Mathieu, col. 1, lines 32-37+}. de Vall shows in Figs. 3a and 3b that resonating circuits can be either series or parallel. Mathieu describes that as the input capacitance of the chip (CS1 in Fig. 5) gets smaller and smaller, a capacitance value CS2 obtained with the screen-printed capacitor 52 is added to compensate (so the overall capacitance stays the same) {see Mathieu, col. 4, lines 22-33+}. Mathieu suggests that it is advantageous to compensate the input capacitance of the chip in

order to obtain perfect resonance. And, with the compensating capacitor on the outside of the chip, perfect resonance can be obtained without having to modify the fabrication process {see Mathieu, column 4, lines 50-55 and paragraph-bridging cols. 4 and 5}. The particular design used by Mathieu is a parallel resonating circuit. With parallel circuits, the total capacitance is $CS_1 + CS_2$ {See Teach Yourself Electricity and Electronics, 2nd Edition, by Stan Gibilisco, page 203}. As CS_1 gets smaller, CS_2 has to get larger to compensate. In a series circuit, the relationship between the two capacitors is $1/CS_2 + 1/CS_1$ {See Teach Yourself Electricity and Electronics, 2nd Edition, by Stan Gibilisco, page 202}. As CS_1 gets smaller, CS_2 must also get smaller to compensate. Therefore, the series relationship is inverse to the parallel relationship. As Mathieu discloses a large capacitor is needed to compensate for the chip capacitor getting smaller {see Mathieu, col. 4, lines 31-33+} and de Vall discloses that either a parallel or series resonator can be used, it would have been obvious to one of ordinary skill in the art, at the time of applicant's invention, to use a series resonator in place of the parallel resonator disclosed by Mathieu because, as taught by Mathieu, the input capacitance of the chip should be compensated in order to obtain perfect resonance. Once this replacement is done, it is inherent that first capacitor C' be smaller than the input capacitance of the IC chip to achieve the same effect (i.e. perfect resonance). Also see Stan Gibilisco, pages 318-319.

In claim 6, de Vall suggests, a second capacitor C connected in parallel with said IC chip 20,

wherein said first capacitance has a capacitance smaller than the sum of the input capacitance of said IC chip and a capacitance of said second capacitor since the first capacitance is smaller than the input capacitance of the IC chip and that the second capacitance, being connected in parallel with said IC chip, has to be greater than the input capacitance of said IC chip. Also see Mathieu, col. 4, lines 31-33.

In claim 10, de Vall teach of a base as shown in Figure 1, wherein said antenna coil (4 or 6) comprises a metallic pattern (i.e. copper layer) formed on said base (i.e. substrate), and any of said capacitors comprises metallic patterns formed on both sides of said base {see de Vall, col. 3, lines 26+}.

In claim 11, de Vall further suggests, said contactless identification comprises an IC card {see de Vall, col. 1, lines 11+}.

In claim 12, de Vall further suggests, said contactless identification comprises a portable terminal {see de Vall, col. 7, lines 26-35}. i.e. credit cards are portable.

In 13, de Vall suggests, that the first capacitor capacitance and an inductance of the antenna coil dominantly determine a resonant frequency of a series circuit including the IC chip, the antenna coil, and the first capacitor as shown in figure 3b.

In claim 14, de Vall suggests, the first capacitor is formed by a metallic pattern (4 and 6) on both sides of the base {see de Vall, Figure 1}.

In claim 15, de Vall suggests, the base is made of a polyimide material (i.e. fleximide substrate) {see de Vall, col. 3, lines 46-49}.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Office Contact Information

11. Please note that the Examiner's supervisor has been changed.
12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to William Bangachon whose telephone number is (571)-272-3065. The Examiner can normally be reached from Monday through Friday, 9:00 AM to 5:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Brian Zimmerman can be reached on (571)-272-3059. The fax phone numbers for the organization where this application or proceeding is assigned is 571-

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273-8300 for regular and After Final formal communications. The Examiner's fax number is **(571)-273-3065** for informal communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.



William L Bangachon
Examiner
Art Unit 2635

April 11, 2007



BRIAN ZIMMERMAN
PRIMARY EXAMINER